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DRAWINGS ATTACHED

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(54) TESTING DIGITAL DATA TRANSMISSION SYSTEMS

(71) We, THE POST OFFICE, a British body corporate established by Statute, of 23 Howland Street, London, W1P 6HQ, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to the testing of digital data transmission systems.

Data transmission systems are usually tested by transmitting a test digital pattern and measuring the errors in the received pattern. The test digital pattern is usually a pseudo-random pattern and errors in the received pattern are detected by generating an identical pseudo-random pattern at the receiver and then comparing this locally-generated pattern with the received pattern. The frames of the received and locally-generated patterns must be correctly phased and, to enable error detection and measurement to be carried out continuously, it is necessary to provide a continuous check on the frame synchronization and means for stopping for the error count when frame slip occurs. These additional requirements increase the complexity of the error detecting equipment.

The present invention provides apparatus for testing a digital data transmission system having a transmitter and a receiver, the transmitter including means operable to generate a serial pattern of digits, in which each digit is a predetermined function of two or more digits each preceding that digit by a particular spacing in the pattern, and to transmit the pattern to the receiver, the receiver including error detecting means operable to compare a digit in the received pattern with the combination, in accordance with the said predetermined function, of the two or more digits preceding that digit by the said particular spacings in the received pattern and to generate an error indication when there is no correlation.

The error detecting means may include means operable to generate, for a digit in the received pattern, a test digit which is the said predetermined function of the two or more digits preceding that digit by the said particular spacings in the received pattern, and means operable to compare that digit with the test digit and to generate an error signal when the compared digits are not the same. The error detecting means need not, however, be operable to generate such a test digit and may, instead, include means operable in any functionally equivalent manner.

The pattern generating means may be operable to generate a pattern of digits in which each digit is the modulo 2 sum of two or more digits each preceding that digit by a particular spacing in the pattern, and the error detecting means is operable to compare a digit in the received pattern with the modulo 2 sum of the two or more digits preceding that digit by the said particular spacings in the received pattern. In one embodiment of the invention, the pattern generating means is operable to generate a pattern of digits in which each digit is the modulo 2 sum of two digits having a predetermined spacing between them and preceding that digit by a particular spacing in the pattern, and the error detecting means is operable to compare a digit in the received pattern with the modulo 2 sum of two digits having the said predetermined spacing between them and preceding that digit by the said particular spacing in the received pattern.

The pattern generating means may include a shift register, and means operable to generate a digit which is the said predetermined function of two or more digits stored in the shift register and to feed the generated digit to the input of the shift register. For example, the pattern generating means may include a shift register having at least n stages ($n > r$), the nth stage and the rth stage each having an output to a modulo 2 adder the output of which is connected to the input of the shift register, the transmitter being operable to transmit the output of the shift register to the receiver. In this case, the error detecting means may include a shift register having at least N stages ($N \geqslant n$), and means operable to compare the input to the $(N-n+1)$th stage with the modula 2 sum of the output of the Nth and $(N - n + r)$th stages.

The invention also provides a method of testing a digital data transmission system, in-

cluding the steps of generating a serial pattern of digits, in which each digit is a predetermined function of two or more digits each preceding that digit by a particular spacing in the pattern, transmitting the pattern to a receiver, and comparing a digit in the received pattern with the combination, in accordance with the said predetermined function, of the two or more digits preceding that digit by the said particular spacings in the pattern.

By way of example, a system in accordance with the invention will be described with reference to the drawings accompanying the Provisional Specification in which:

Fig. 1 is a diagram of pseudo-random pattern generating apparatus forming part of the system, and

Fig. 2 is a diagram of error detecting apparatus forming part of the system.

The drawings illustrate apparatus for detecting errors in a binary digital data transmission system. A pseudo-random pattern if binary data is generated in the apparatus illustrated in Fig. 1 and is passed from the transmitter to the receiver of the system that is being tested. Errors in the received pattern are detected in the apparatus illustrated in Fig. 2, thereby enabling the probability of bit error in the transmission system to be measured.

The pseudo-random pattern generator (Fig. 1) is of conventional form and includes a shift register SRI having n stages SR1, SR2, ... SRr, ... SRn. The rth and nth stages of the register SRI have outputs to a modulo 2 adder ADD1 the output of which is connected back to the input of the register. The output of the register is transmitted over the system that is being tested.

When a suitable train of bits is stored in the shift register SRI the apparatus functions to generate a pseudo-random pattern of bits in which, under conditions of no error, any bit is correlated with the modulo 2 sum of the rth and nth preceding bits. The function of the register SRI is illustrated, by way of example, for the case $n = 4$ in the Table I set out below. In this Table it is assumed that the third and fourth stages of the register are connected to the input of the modulo 2 adder ADD1 and that, initially, the digits stored in the stages SR1—SR4 of the register are 1, 0, 0, 1 respectively as shown in Table I. The bits "0" and "1" stored in stages SR3 and SR4 of the register are combined in the adder ADD1 to yield a bit "1" which is fed to the shift register input.

The register is advanced by pulses from a clock source and, on receipt of the first advance pulse the bits stored in register stages SR1, SR2 and SR3 are fed to stages SR2, SR3 and SR4 respectively, and the bit "1" from the modulo 2 adder is fed to register stage SR1 Bits "0" and "0" which are now stored in register stages SR3 and SR4 are combined in the adder ADD1 to yield a bit "0" which is fed to the register input. Upon receipt of the next advance pulse the process is repeated, and it will be seen that in the resultant output pattern (once the pattern is established) each bit is the modulo 2 sum of the third and fourth preceding bits, unless an error has been introduced.

TABLE I

Shift Register SRI				ADD1 Output	Shift Register (SRI) Output
SR1	SR2	SR3	SR4		
1	0	0	1	1	1
1	1	0	0	0	0
0	1	1	0	1	0
1	0	1	1	0	1
0	1	0	1	1	1
1	0	1	0	1	0
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	0	1
0	1	1	1	0	1
0	0	1	1	0	1
0	0	0	1	1	1
1	0	0	0	0	0
0	1	0	0	0	0
0	0	1	0	1	0
1	0	0	1	1	1
					etc.

The use of a four stage shift register has been described by way of example only and it will be appreciated that registers having other numbers of stages could be employed and also that the inputs to the adder ADD1 need not be from adjacent register stages.

The error detecting apparatus (Fig. 2) also includes a shift register SRII, but this register has, for a purpose which will be explained below, (n + 1) stages: SR1, SR2 . . . . . SRr, SR(r + 1) . . . . . SRn, SR(n + 1). The (r+1)th and the (n+1)th stages have outputs to a modulo 2 adder ADD2 the output of which is applied, together with the output of the first stage of the register, to a correlator CLTR (for example, a further modulo 2 adder). The correlator compares the inputs and generates an output signal when the inputs are not the same.

The pseudo-random pattern from the apparatus of Fig. 1 is fed (in the form in which it is received at the receiver of the transmission system) to the shift register SRII. Under conditions of no error, the modulo 2 sum of the digits which at any one time are stored in stage SR(r + 1) and SR(n + 1) of register SRII should correlate with the digit stored in the first stage of the register, since this was the manner in which the pattern was generated in the apparatus of Fig. 1. If there is no correlation an error is present, and an output signal is generated by the correlator CLTR.

The use of n + 1 stages in the shift register SRII is not essential: a register having n stages could be used, with the adder ADD2 receiving the output of the rth and nth stages (instead of the (r + 1)th and (n + 1)th stages) and with the input to the register (instead of the output of the first stage) being applied to the correlator CLTR. In such an arrangement, however, it is advisable to include a buffer

stage between the input to the register SRII and the correlator CLTR to ensure that no distorted pulses are fed to the correlator. When a register SII having (n+1) stages is used, the first stage of the register itself acts as a buffer stage to ensure that undistorted, correctly clocked signals are fed to the correlator.

The particular arrangement of error detecting gates (that is, modulo 2 adder ADD2 and correlator CLTR) shown in Fig. 2 is not the only arrangement that could be utilized to detect errors in a digital pattern generated in the apparatus of Fig. 1. Other gating arrangements having the same functional effect as the gates ADD2 and CLTR (that is, the comparison of the output of the first stage of the shift register SRII with the modulo 2 sum of the outputs of the $(r+1)$th and $(n+1)$th stages) could be employed.

The function of the error-detecting apparatus shown in Fig. 2 is illustrated, by way of example, in Tables II and III set out below. In this case, it is assumed that the apparatus is to be employed with pattern generating apparatus as described above with reference to Table I. Accordingly since $n=4$, the shift register SR11 has 5 stages, the fourth and fifth stages having outputs to the modulo 2 adder ADD2. It is also assumed that the shift register SR1 generates the output pattern specified in Table I.

TABLE II

Shift Register SRII Input	Shift Register SRII					ADD2 Output
	SR1	SR2	SR3	SR4	SR5	
0	1	1	0	0	1	1
1	0	1	1	0	0	0
0	1	0	1	1	0	1
1	0	1	0	1	1	0
1	1	0	1	0	1	1
1	1	1	0	1	0	1
1	1	1	1	0	1	1
0	1	1	1	1	0	1
0	0	1	1	1	1	0
0	0	0	1	1	1	0
1	0	0	0	1	1	0
0	1	0	0	0	1	1
0	0	1	0	0	0	0
1	0	0	1	0	0	0
1	1	0	0	1	0	1
					etc.	

Table II illustrates the function of the error detecting apparatus in the absence of bit error. When the first bit from the output of shift register SRI, which is a "1" reaches the fifth stage of register SRII, the following "0" is in the fourth stage so that the output of the modulo 2 adder is a bit "1". This is compared by the correlator CLTR with the bit stored in the first stage of register SRII, which as shown in Table II is in the absence of errors, also a "1". The correlator, accordingly, does not generate an error signal.

The register SRII is advanced by pulsest from a clock source and, on receipt of the next advance pulse, the bits stored in stages SR1 to SR4 of register SRII are fed to stages SR2 to SR5 and the next bit in the pattern generated by the Fig. 1 apparatus is fed to stage SR1. As shown in Table II, there is now a "0" in each of stages SR4 and SR5 so that the adder ADD2 yields the bit "0". The bit stored in stage SR1 of the register is now also a "0" so that the correlator CLTR again produces no output.

TABLE III

Shift Register SRII Input	Shift Register SRII					Add 2 Output
	SR1	SR2	SR3	SR4	SR5	
0	1	1	0	0	1	1
$0(e_1)$	0	1	1	0	0	0
0	$0(e_1)$	0	1	1	0	1 Error
1	0	$0(e_1)$	0	1	1	0
1	1	0	$0(e_1)$	0	1	1
1	1	1	0	$0(e_1)$	0	0 Error
$0(e_2)$	1	1	1	0	$0(e_1)$	0 Error
0	$0(e_2)$	1	1	1	0	1 Error
0	0	$0(e_2)$	1	1	1	0
0	0	0	$0(e_2)$	1	1	0
1	0	0	0	$0(e_2)$	1	1 Error
0	1	0	0	0	$0(e_2)$	0 Error
0	0	1	0	0	0	0
1	0	0	1	0	0	0
1	1	0	0	1	0	1 etc.

Table III indicates the function of the error detector when two bits in the data pattern are received incorrectly as "0" instead of "1". The errors are indicated in Table III by the symbols (e_1) and (e_2). When the first error (e_1) reaches the stage SR1 of the register, there is a bit "1" stored in the stage SR4 and a bit "0" stored in the stage SR5 so that the output of adder ADD2 is a bit "1". At this time the error bit "0" is stored in stage SR1 of the register so that there is no correlation between the inputs to the correlator CLTR which therefore produces an error signal.

It can be seen from a consideration of Table III that, provided the errors are so widely spaced that there is only one bit error in the register SRII at a time, each error will cause the correlator to generate three error signals (resulting from the passage of the error through stages SR1, SR4 and SR5 of the register). In view of this, the error detector includes, in addition to the correlator CLTR, a divide by three circuit DIV which generates an output signal in response to every three error signals generated by the correlator. The output of the divide circuit DIV is fed to a counter (not shown) to obtain a measurement of the bit error rate in the transmission system. Alternatively, the production of three error signals by a single error could be eliminated by including a modulo 2 adder between stages SR1 and SR2 in the shift register SRII and applying the output of the correlator CLTR to this adder together with the received pattern from the shift register stage SR1. The generation of an error signal by the correlator CLTR will then result in correction of the erroneous input digit to the shift register stage SR2

with the result that no further error signals will be caused by that digit.

It can be shown, if the bit errors in the pattern received by the Fig. 2 apparatus are assumed to be statically independent, that the bit error rate as measured at the output of the divide circuit DIV (that is, the mean error rate approximates very closely to the actual rate when the probability of bit error is low: for example, the measurement accuracy is about 98% for a bit error probability of 0.01, dropping to about 60% for a bit error probability of 0.25. These measurement accuracies are comparable (except at very high error rates) with those that can be achieved with conventional error detector involving the local generation (at the receiver) of a test pattern and comparison of the test and received patterns. However, conventional detectors involve complex equipment to synchronize the test and received patterns and may lose synchronization at high error rates whereas apparatus of the type shown in Fig. 2 provides a continuously synchronized error detector which is not affected by error rate.

If bit errors occur in blocks, instead of singly as assumed in Table III, then the measurement accuracy may be reduced. This is illustrated in Table IV which is similar to Table II and III but includes a block of three bit errors (e_1), (e_2) and (e_3).

TABLE IV

Shift Register (SRII) Input	Shift Register (SRII)					ADD2 Output
	SR1	SR2	SR3	SR4	SR5	
$1(e_1)$	1	1	0	0	1	1
$0(e_2)$	$1(e_1)$	1	1	0	0	0 Error
$1(e_3)$	$0(e_2)$	$1(e_1)$	1	1	0	1 Error
1	$1(e_3)$	$0(e_2)$	$1(e_1)$	1	1	0 Error
1	1	$1(e_3)$	$0(e_2)$	$1(e_1)$	1	0 Error
1	1	1	$1(e_3)$	$0(e_2)$	$1(e_1)$	1
1	1	1	1	$1(e_3)$	$0(e_2)$	1
0	1	1	1	1	$1(e_3)$	0 Error
0	0	1	1	1	1	0
0	0	0	1	1	1	0
1	0	0	0	1	1	0
0	1	0	0	0	1	1
0	0	1	0	0	0	0
1	0	0	1	0	0	0
1	1	0	0	1	0	1

Since the presence of one error sometimes cancels out the presence of another, only five error signals are generated by the correlator CLTR whereas nine signals would have been generated if the errors had passed through the register SRII singly. A similar effect may occur if the spacing between bit errors is, for example, (referring to Figs. 1 and 2) r or n or n-r.

It has been found that blocks of statistically-independent errors do not have a significant effect on the accuracy of the long-term mean error rate as measured at the output of the divide circuit DIV (Fig. 2), but if it is wished to measure the block errors themselves then measurement accuracy can be increased (at least as regards bit errors occurring in blocks of two) by spacing the rth and nth stages

of the registers SRI, SRII apart by at least one stage. As the spacing between the rth and nth stages, and also the value of r is increased further, so the apparatus becomes more alert to longer blocks of bit errors.

A further advantage of spacing the rth and nth stages of registers SRI, SRII apart by at least one stage is that errors occurring in coherent pairs can be detected. Coherent pairs of errors are errors which occur simultaneously in adjacent bits of a digital stream and are not statistically independent. Such errors can arise when the digital stream is transmitted by modulation onto a carrier, depending on the method of modulation/demodulation that is used. One method which can give rise to coherent pairs of errors is phase coherent modulation/demodulation with differential coding/decoding: in this system, the phase of any one bit is compared with the phase of the previous bit with the result that a single error in the coded pulse stream causes simultaneous errors in adjacent bits of the decoded pulse stream. It has been found that apparatus as shown in Figs 1 and 2 (with $(n - r) > 1$) can detect these coherent pairs of errors with similar accuracy to that associated with the detection of single errors, and as the spacing $(n - r)$ is increased so the apparatus becomes more alert to errors in larger coherent blocks.

It will be appreciated from the above description that the form of the error detecting apparatus is dependent upon the form of the pseudo-random pattern transmitted over the system, and that the arrangement shown in Fig. 1 could be replaced by other pseudo-random pattern generators with appropriate modifications being made to the detector of Fig. 2. The general arrangement shown in the drawing is, however, preferable on the ground of simplicity, particularly advantageous arrangements (as regards the detection of block errors) being those in which the pattern generator (Fig. 1) has 9 stages with a modulo 2 feed back from stages 5 and 9 (i.e. $n = 9$, $r = 5$) and 18 stages with a modulo 2 feed back from stages 11 and 18 (i.e. $n=18$, $r=11$).

WHAT WE CLAIM IS:—

1. Apparatus for testing a digital data transmission system having a transmitter and a receiver, the transmitter including means operable to generate a serial pattern of digits, in which each digit is a predetermined function of two or more digits each preceding that digit by a particular spacing in the pattern, and to transmit the pattern to the receiver, the receiver including error detecting means operable to compare a digit in the received pattern with the combination, in accordance with the said predetermined function, of the two or more digits preceding that digit by the said particular spacings in the received pattern and to generate an error indication when there is no correlation.

2. Apparatus as claimed in claim 1, in which the error detecting means includes means operable to generate, for a digit in the received pattern, a test digit which is the said predetermined function of the two or more digits preceding that digit by the said particular spacings in the received pattern, and means operable to compare that digit with the test digit and to generate an error signal when the compared digits are not the same.

3. Apparatus as claimed in claim 1 or claim 2, in which the pattern generating means is operable to generate a pattern of digits in which each digit is the modulo 2 sum of two or more digits each preceding that digit by a particular spacing in the pattern, and the error detecting means is operable to compare a digit in the received pattern with the modulo 2 sum of the two or more digits preceding that digit by the said particular spacings in the received pattern.

4. Apparatus as claimed in any one of the preceding claims, in which the pattern generating means includes a shift register, and means operable to generate a digit which is the said predetermined function of two or more digits stored in the shift register and to feed the generated digit to the input of the shift register.

5. Apparatus as claimed in any one of the preceding claims, in which the pattern generating means is operable to generate a pattern of digits in which each digit is the modulo 2 sum of two digits having a predetermined spacing between them and preceding that digit by a particular spacing in the pattern, and the error detecting means is operable to compare a digit in the received pattern with the modulo 2 sum of two digits having the said predetermined spacing between them and preceding that digit by the said particular spacing in the received pattern.

6. Apparatus as claimed in any one of the preceding claims, in which the pattern generating means includes a shift register having at least n stages $(n > r)$, the nth and the rth stage each having an output to a modulo 2 adder the output of which is connected to the input of the shift register, the transmitter being operable to transmit the output of the shift register to the receiver.

7. Apparatus as claimed in claim 6, in which the error detecting means includes a shift register having at least N stages $(N \geqslant n)$, and means operable to compare the input to the $(N-n+1)$th stage with the modulo 2 sum of the output of the Nth and $(N - n + r)$th stages.

8. Apparatus as claimed in claim 7, in which the Nth stage and the $(N - n + r)$th stage of the error detecting shift register each has an output to a modulo 2 adder, and the error detecting means includes means operable to compare the output of that modulo 2 adder with the input to the $(N - n + 1)$th stage of the error detecting shift register.

9. Apparatus as claimed in claim 7 or claim 8, in which the Nth stage of the error detecting shift register is the $(n + 1)$th stage.

10. Apparatus as claimed in any one of claims 7 to 9, in which the error detecting means is operable to generate an error signal in response to every third occurrence of no correlation between the input to the $(N - n + 1)$th stage of the error detecting shift register and the modulo 2 sum of the output of the Nth and $(N-n+r)$th stages.

11. Apparatus as claimed in any one of claims 6 to 10, in which the nth stage and the rth stage of the shift register(s) are spaced apart by at least one stage.

12. Apparatus as claimed in any one of claims 6 to 11, in which the nth and rth stages of the shift register(s) are the 9th and 5th stages respectively.

13. Apparatus as claimed in any one of claims 6 to 11, in which the nth and rth stages of the shift register(s) are the 18th and 11th stages respectively.

14. Apparatus for testing a digital data transmission system, substantially as described herein with reference to and as illustrated by the drawings accompanying the Provisional Specification.

15. A method of testing a digital data transmission system, including the steps of generating a serial pattern of digits, in which each digit is a predetermined function of two or more digits each preceding that digit by a particular spacing in the pattern, transmitting the pattern to a receiver, and comparing a digit in the received pattern with the combination, in accordance with the said predetermined function, of the two or more digits preceding that digit by the said particular spacings in the pattern.

16. A method as claimed in claim 15, in which the said two or more digits are combined to produce a test digit which is the predetermined function of those digits.

17. A method as claimed in claim 15 or claim 16, including the step of generating an error indication when there is no correlation between the compared digit and the said combination.

18. A method according to any one of claims 15 to 17, substantially as described herein with reference to the drawings accompanying the Provisional Specification.

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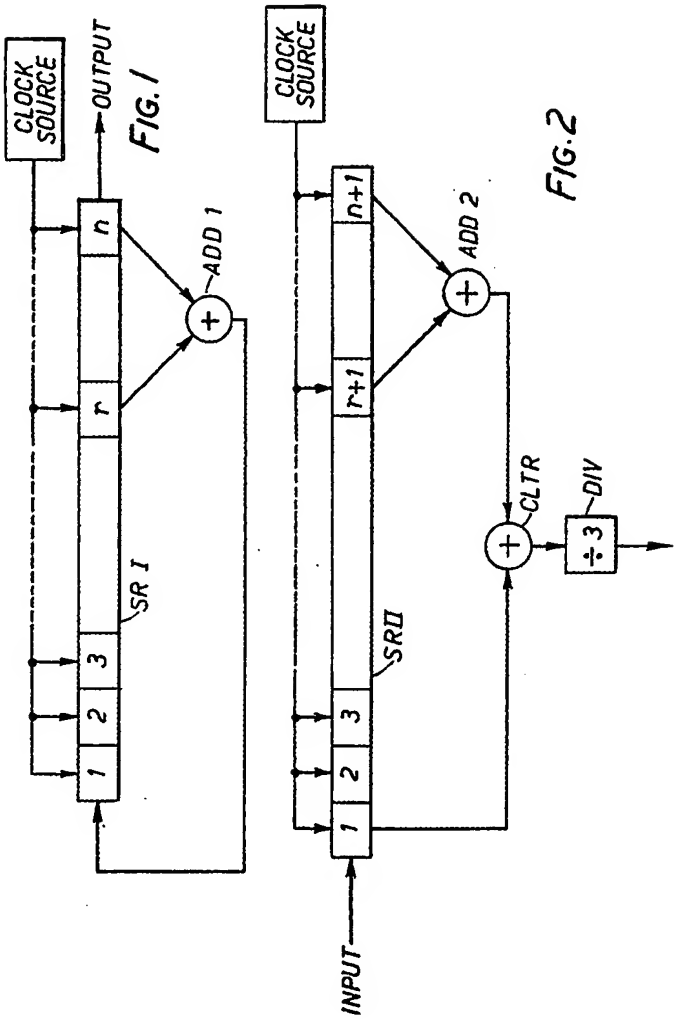
CLOCK SOURCE
OUTPUT
n
r
3
2
1
ADD 1
SR I

FIG. 1

CLOCK SOURCE
n+1
r+1
3
2
1
ADD 2
SR II
CLTR
DIV
÷ 3
INPUT

FIG. 2